Abstract of the Disclosure

The present invention relates to a method for fabricating a semiconductor device. In more detail of the aforementioned method, a first mask layer covering a cell region is formed on an insulation layer in the cell region. Meanwhile, a second mask layer is formed in a peripheral circuit region with a predetermined distance from the first mask layer. The insulation layer is then etched with use of the first and the second mask layers as an etch mask to form a spacer at both sidewalls of each gate line pattern in the peripheral region and simultaneously form a guard beneath the second mask layer. The first and the second mask layers are removed thereafter. Next, a third mask layer opening the cell region but covering the whole regions including a guard region in the peripheral circuit region is formed. A wet etching process is performed to the insulation layer remaining in the cell region by using the third mask layer as an etch mask.